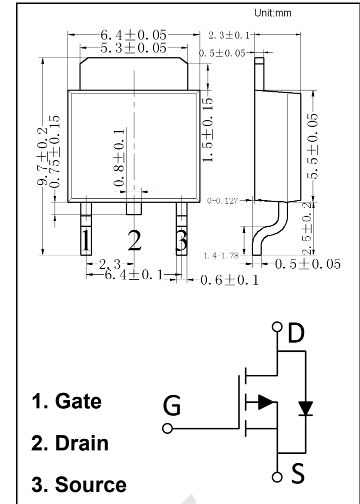
SHENZHEN LONG JING MICRO-ELECTRONICS CO., LTD.

TO-252 Plastic-Encapsulate MOSFETS

7P20G P-Channel MOSFET



Features

- $R_{DS(ON)} \leq 0.69\Omega$ @V_{GS} = -10V
- Ultra low gate charge (typical 19nC)
- Low reverse transfer capacitance (C_{RSS} = typical 25pF)
- Fast switching capability
- Avalanche energy specified
- Improved dv/dt capability, high ruggedness

Applications

The 7P20 uses advanced proprietary, planar stripe, DMOS technology to provide excellent RDS(ON), low gate charge and operation with low gate voltages. This device is suitable for use as a load switch or in PWM applications. They are also well suited for high efficiency switching DC/DC converters.

Maximum Ratings (T_C=25°C unless otherwise specified)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain-Source voltage		-200	V
V_{GSS}	Gate-Source voltage		±30	
I_D	Continuous Drain Current		-5.7	A
I_{DM}	Pulsed Drain Current 2)		-22.8	
I_{AR}	Avalanche Current 2)		-5.7	A
E_{AS}	Single Pulsed Avalanche Energy 3)		570	mJ
E_{AR}	Repetitive Avalanche Energy 2)		5.5	mJ
dv/dt	Peak Diode Recovery dv/dt 4)		-5.5	V/ns
P_D	Maximum Power Dissipation 1)	T_a = 25°C	2.5	W
		T_c = 25°C	55	
T_J	Junction Temperature		+150	°C
T_{STG}	Storage Temperature		-55 to 150	°C

Notes

1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.
   Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Pulse width limited by $T_{J(MAX)}$
3. L=26.3mH, I_{AS}=-5.7A, V_{DD}=-50V, R_G=25Ω
4. $I_{SD} \leqq$-7.3A, di/dt≦300A/μs, $V_{DD} \leqq BV_{DSS}$

Thermal Data

Symbol	Parameter	Max	Unit
$R_{θJA}$	Junction-to-Ambient	110	°C/W
$R_{θJC}$	Junction-to-Case	2.27	

Electrical Characteristics (T_c=25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ [1]	Max	Unit
Off Characteristics						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = -250μA	-200			V
$\Delta BV_{DSS} / \Delta T_J$		I_D=-250μA, Referenced to25°C		-0.1		V/°C
I_{GSS}	Gate-body Leakage current	V_{DS} = 0V, V_{GS} = ±30V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -200V, V_{GS} = 0V			-1	μA
On Characteristics						
$V_{GS(th)}$	Gate-Threshold Voltage	V_{DS} = V_{GS}, I_D = -250μA	-3.0		-5.0	V
$R_{DS(on)}$	Drain-Source On-Resistance	V_{GS} = -10V, I_D = -2.85A		0.54	0.69	Ω
g_{fs}	Forward Transconductance [1]	V_{DS} = -40V, I_D = -2.85A		3.7		S
Dynamic Parameters						
C_{iss}	Input Capacitance	V_{GS} = 0V V_{DS} = -25V f = 1.0MHz		590	770	pF
C_{oss}	Output Capacitance			140	180	
C_{rss}	Reverse Transfer Capacitance			25	35	
Switching Parameters						
Q_g	Total Gate Charge	V_{GS} = -10V, I_D = -7.3A, V_{DS} = -160V [1,2]		19	25	nC
Q_{gs}	Gate-Source Charge			4.6		
Q_{gd}	Gate-Drain Charge			9.5		
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -100V, I_D = -7.3A, R_G = 25Ω [1, 2]		15	40	ns
t_R	Turn-On Rise Time			110	230	
$t_{d(off)}$	Turn-Off Delay Time			30	70	
t_F	Turn-Off Fall Time			42	90	
Source- Drain Diode Ratings and Characteristics						
V_{SD}	Diode Forward Voltage	I_S = -5.7A, V_{GS} = 0V			-5.0	V
I_S	Maximum Body-Diode Continuous Current				-5.7	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				-22.8	A
t_{RR}	Body Diode Reverse Recovery Time	V_{GS} = 0V, I_S = -7.30A dI_F/dt = 100A/s [1]		180		ns
Q_{RR}	Body Diode Reverse Recovery Charge			1.07		μC

Notes:

1. Pulse Test : Pulse width≦300μs, Duty cycle≦2%
2. Essentially independent of operating temperature

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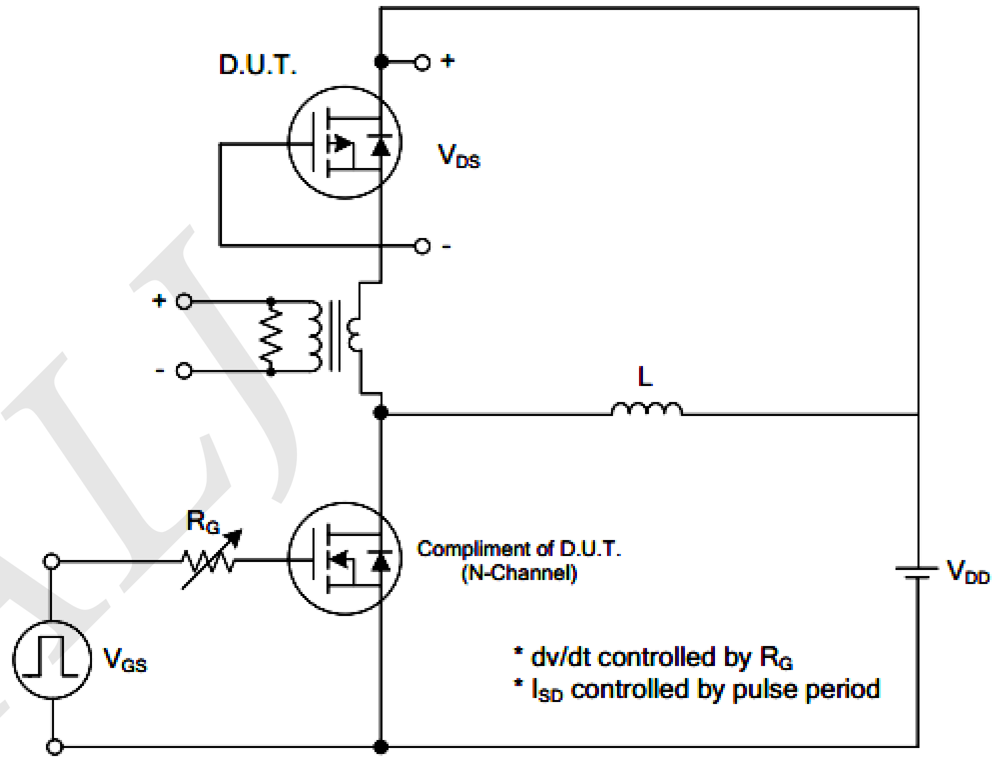

Fig. 1A Peak Diode Recovery dv/dt Test Circuit

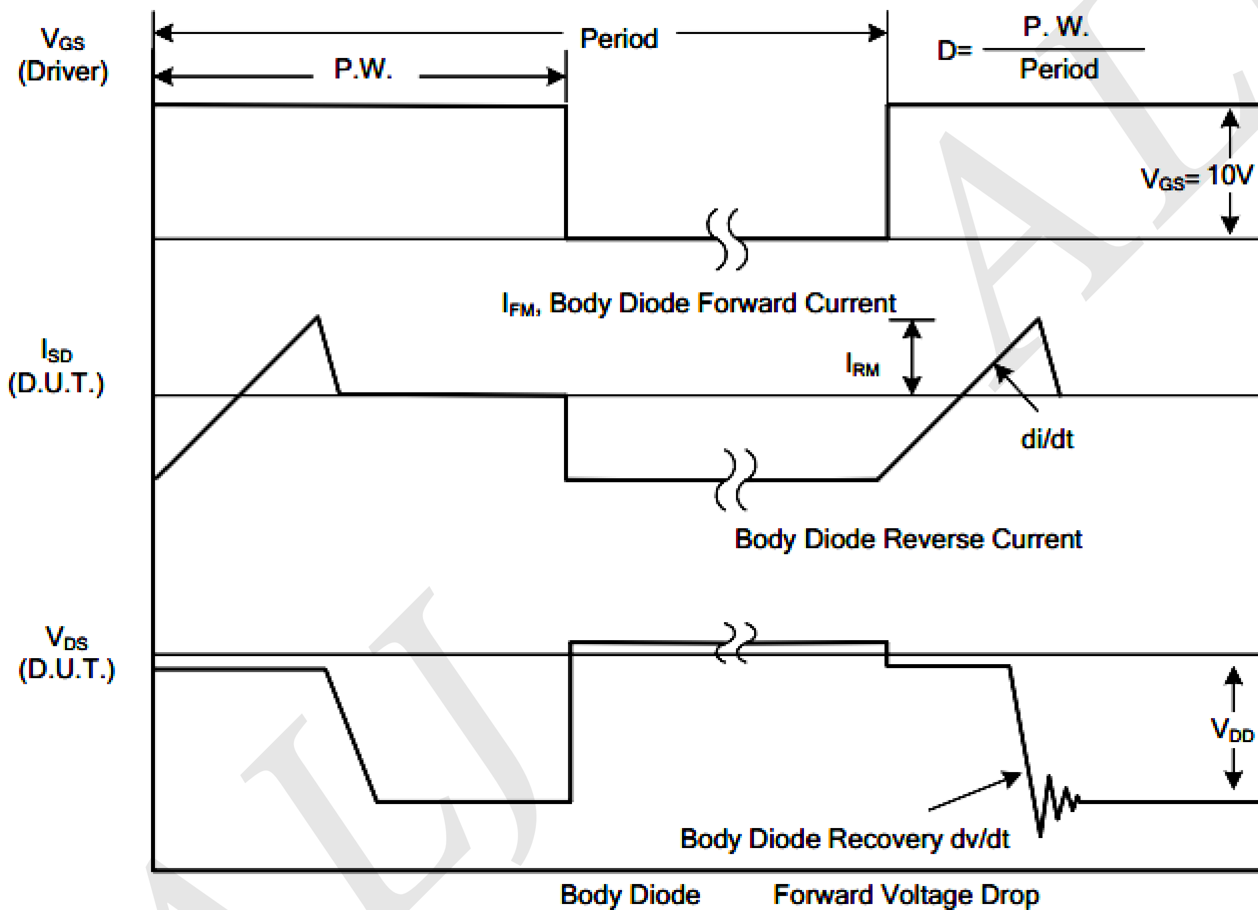

Fig. 1B Peak Diode Recovery dv/dt Waveforms

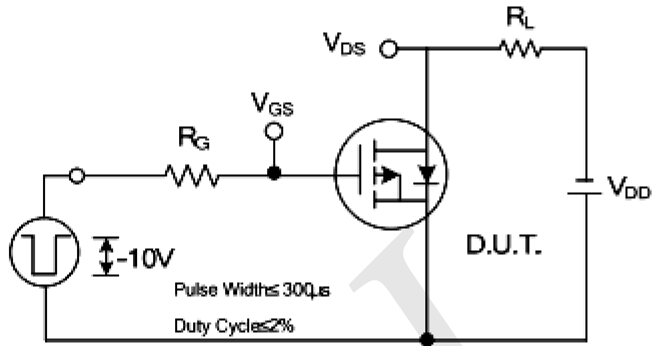

Fig. 2A Switching Test Circuit

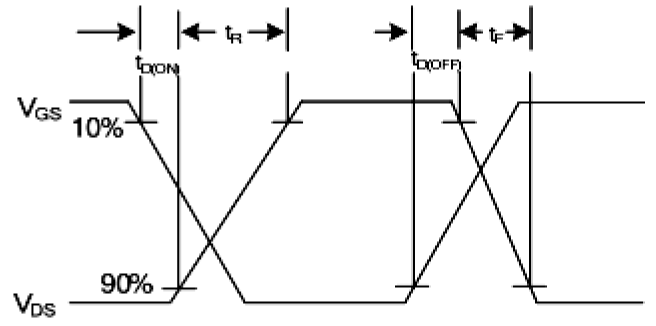

Fig. 2B Switching Waveforms

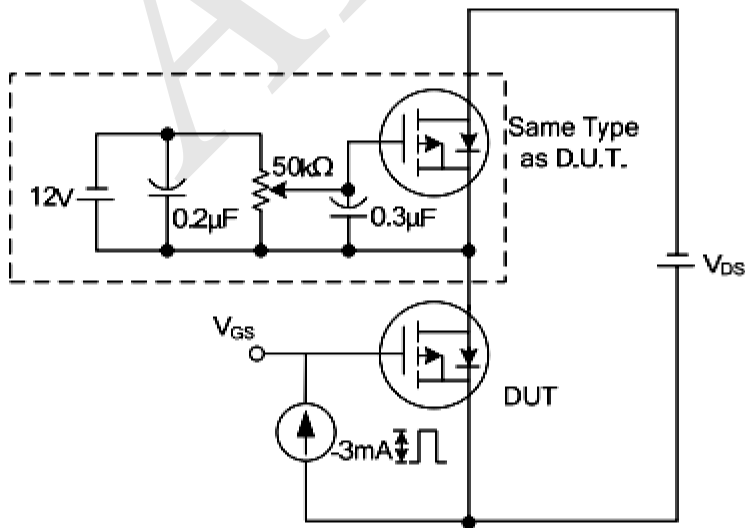

Fig. 3A Gate Charge Test Circuit

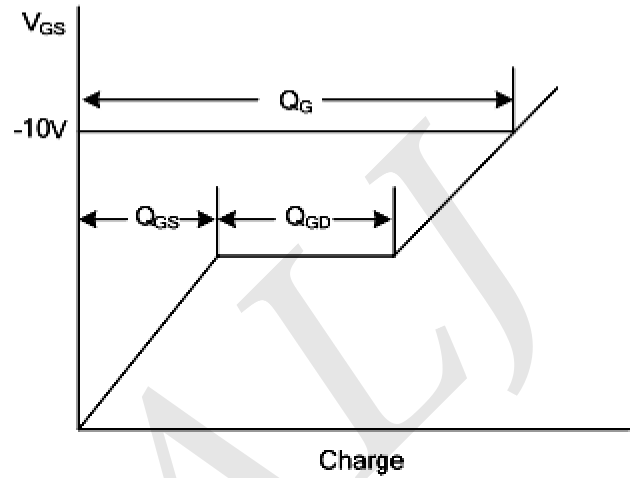

Fig. 3B Gate Charge Waveform

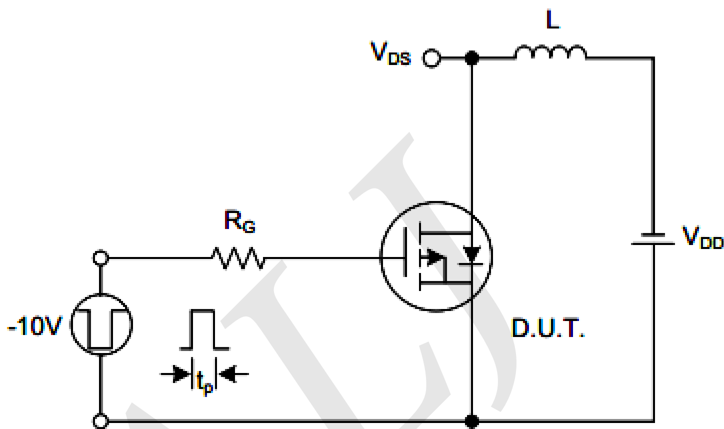

Fig. 4A Unclamped Inductive Switching Test Circuit

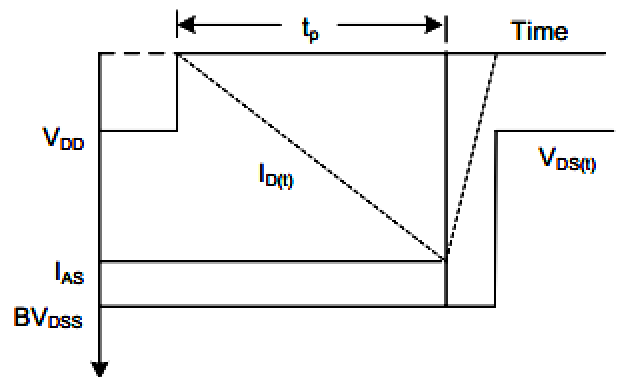

Fig. 4B Unclamped Inductive Switching Waveforms